

SignalCore™

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User Manual

SC5312A & SC5313A

6 GHz Direct IQ Demodulator

www.signalcore.com

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1 General Information

1.1 Warranty

This product is warranted against defects in materials and workmanship for a period of three years from the date of shipment. SignalCore will, at its option, repair or replace equipment that proves to be defective during the warranty period. This warranty includes parts and labor.

Before any equipment will be accepted for warranty repair or replacement, a Return Material Authorization (RMA) number must be obtained from a SignalCore customer service representative and clearly marked on the outside of the return package. SignalCore will pay all shipping costs relating to warranty repair or replacement.

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鉛 Lead (Pb)	汞 Mercury (Hg)	镉 Cadmium (Cd)	六价铬 Hexavalent Chromium (Cr(VI))	多溴联苯 Polybrominated biphenyls (PBB)	多溴二苯醚 Polybrominated diphenyl ethers (PBDE)
✓	✓	✓	✓	✓	✓

A ✓ indicates that the hazardous substance contained in all of the homogeneous materials for this product is below the limit requirement in SJ/T11363-2006. An X indicates that the particular hazardous substance contained in at least one of the homogeneous materials used for this product is above the limit requirement in SJ/T11363-2006.

1.4 CE European Union EMC & Safety Compliance Declaration

The European Conformity (CE) marking is affixed to products with input of 50 - 1,000 Vac or 75 - 1,500 Vdc and/or for products which may cause or be affected by electromagnetic disturbance. The CE marking symbolizes conformity of the product with the applicable requirements. CE compliance is a manufacturer’s self-declaration allowing products to circulate freely within the European Union (EU). SignalCore products meet the essential requirements of Directives 2004/108/EC (EMC) and 2006/95/EC (product safety) and comply with the relevant standards. Standards for Measurement, Control and Laboratory Equipment include EN 61326 and EN 55011 for EMC, and EN 61010-1 for product safety.

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- (1) PRODUCTS FOR SALE BY SIGNALCORE, INCORPORATED ARE NOT DESIGNED WITH COMPONENTS NOR TESTED FOR A LEVEL OF RELIABILITY SUITABLE FOR USE IN OR IN CONNECTION WITH SURGICAL IMPLANTS OR AS CRITICAL COMPONENTS IN ANY LIFE SUPPORT SYSTEMS WHOSE FAILURE TO PERFORM CAN REASONABLY BE EXPECTED TO CAUSE SIGNIFICANT INJURY TO A HUMAN.

- (2) IN ANY APPLICATION, INCLUDING THE ABOVE, RELIABILITY OF OPERATION OF THE SOFTWARE PRODUCTS CAN BE IMPAIRED BY ADVERSE FACTORS, INCLUDING BUT NOT LIMITED TO FLUCTUATIONS IN ELECTRICAL POWER SUPPLY, COMPUTER HARDWARE MALFUNCTIONS, COMPUTER OPERATING SYSTEM SOFTWARE FITNESS, FITNESS OF COMPILERS AND DEVELOPMENT SOFTWARE USED TO DEVELOP AN APPLICATION, INSTALLATION ERRORS, SOFTWARE AND HARDWARE COMPATIBILITY PROBLEMS, MALFUNCTIONS OR FAILURES OF ELECTRONIC MONITORING OR CONTROL DEVICES, TRANSIENT FAILURES OF ELECTRONIC SYSTEMS (HARDWARE AND/OR SOFTWARE), UNANTICIPATED USES OR MISUSES, OR ERRORS ON THE PART OF THE USER OR APPLICATIONS DESIGNER (ADVERSE FACTORS SUCH AS THESE ARE HEREAFTER COLLECTIVELY TERMED "SYSTEM FAILURES"). ANY APPLICATION WHERE A SYSTEM FAILURE WOULD CREATE A RISK OF HARM TO PROPERTY OR PERSONS (INCLUDING THE RISK OF BODILY INJURY AND DEATH) SHOULD NOT BE SOLELY RELIANT UPON ANY ONE COMPONENT DUE TO THE RISK OF SYSTEM FAILURE. TO AVOID DAMAGE, INJURY, OR DEATH, THE USER OR APPLICATION DESIGNER MUST TAKE REASONABLY PRUDENT STEPS TO PROTECT AGAINST SYSTEM FAILURES, INCLUDING BUT NOT LIMITED TO BACK-UP OR SHUT DOWN MECHANISMS. BECAUSE EACH END-USER SYSTEM IS CUSTOMIZED AND DIFFERS FROM SIGNALCORE'S TESTING PLATFORMS, AND BECAUSE A USER OR APPLICATION DESIGNER MAY USE SIGNALCORE PRODUCTS IN COMBINATION WITH OTHER PRODUCTS IN A MANNER NOT EVALUATED OR CONTEMPLATED BY SIGNALCORE, THE USER OR APPLICATION DESIGNER IS ULTIMATELY RESPONSIBLE FOR VERIFYING AND VALIDATING THE SUITABILITY OF SIGNALCORE PRODUCTS WHENEVER SIGNALCORE PRODUCTS ARE INCORPORATED IN A SYSTEM OR APPLICATION, INCLUDING, WITHOUT LIMITATION, THE APPROPRIATE DESIGN, PROCESS AND SAFETY LEVEL OF SUCH SYSTEM OR APPLICATION.

2 Physical Description

2.1 Unpacking

All SignalCore products ship in antistatic packaging (bags) to prevent damage from electrostatic discharge (ESD). Under certain conditions, an ESD event can instantly and permanently damage several of the components found in SignalCore products. Therefore, to avoid damage when handling any SignalCore hardware, you must take the following precautions:



1. Ground yourself using a grounding strap or by touching a grounded metal object.
2. Touch the antistatic bag to a grounded metal object before removing the hardware from its packaging.
3. **NEVER touch exposed signal pins.** Due to the inherent performance degradation caused by ESD protection circuits in the RF path, the device has minimal ESD protection against direct injection of ESD into the RF signal pins.
4. When not in use, store all SignalCore products in their original antistatic bags.

Remove the product from its packaging and inspect it for loose components or any signs of damage. Notify SignalCore immediately if the product appears damaged in any way.

2.2 Setting Up the Device

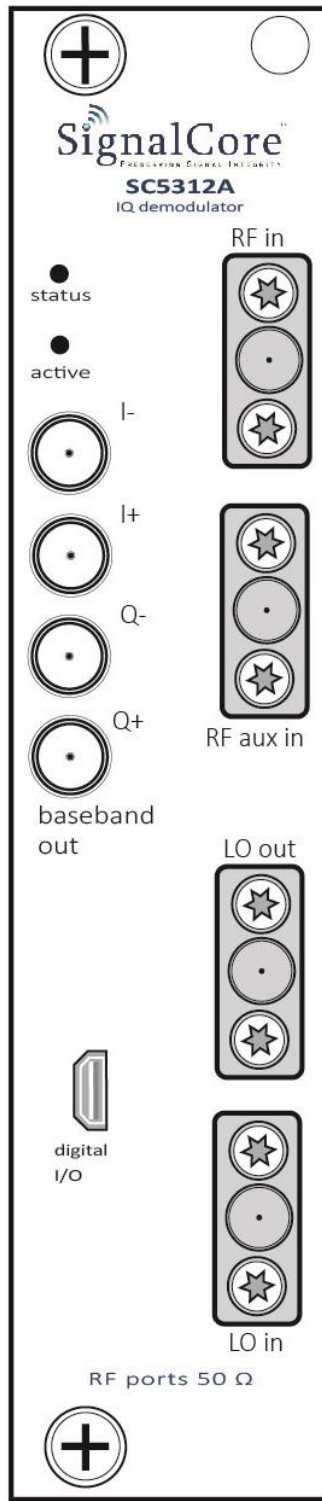
Integration of the SC5312A and SC5313A modules requires attention to maintain effective cooling. Inadequate cooling can cause the temperature inside the RF housing to rise above the maximum for this product, leading to improper performance, reduction of product lifespan or complete product failure. SignalCore suggests providing either moderate airflow across the RF housing, or if active cooling is not an option, using thermal interface materials to bond the RF housing to a larger heatsinking surface (i.e. a system enclosure). As each system configuration into which the device is integrated is unique, detailed cooling options cannot be provided.



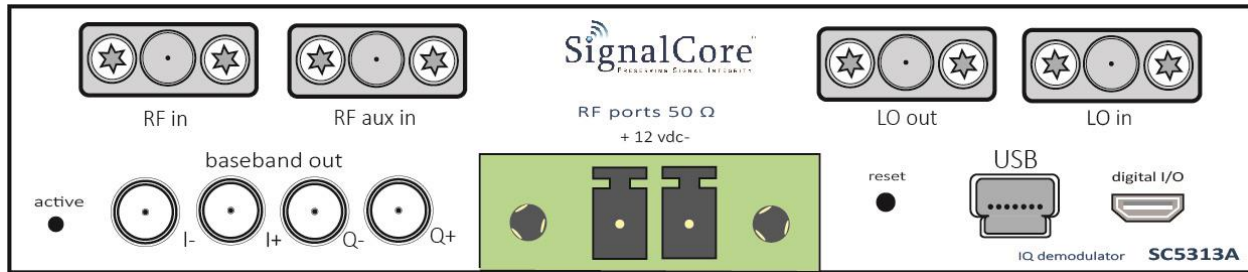
A cooling plan is sufficient when the SC5312A and SC5313A on-board temperature sensors indicate a rise of no more than 20°C above ambient temperature under normal operating conditions.

2.3 Front Interface Indicators and Connectors

The SC5312A is a PXIe-based RF downconverter with all user I/O located on the front face of the module as shown below.



The SC5313A is a core module-based IQ demodulator with all I/O connections and indicators located on the front face of the module as shown below.



2.3.1 Power Connection

Power to the SC5313A is provided to the device through a two-position screw terminal block connection. Proper operation of the device requires a +12 VDC source and ground return wires capable of delivering a minimum current of 1.5 amps. The polarity of the connector is shown on the front panel of the RF module, just above the screw terminal block.

2.3.2 Signal Connections

All signal connections (ports) on the device are SMA-type. Exercise caution when fastening cables to the signal connections. Over-tightening any connection can cause permanent damage to the device.

! *The condition of your system signal connections can significantly affect measurement accuracy and repeatability. Improperly mated connections or dirty, damaged, or worn connectors can degrade measurement performance. Clean out any loose, dry debris from connectors with clean, low-pressure air (available in spray cans from office supply stores).*

If deeper cleaning is necessary, use lint-free swabs and isopropyl alcohol to gently clean inside the connector barrel and the external threads. Do not mate connectors until the alcohol has completely evaporated. Excess liquid alcohol trapped inside the connector may take several days to fully evaporate and may degrade measurement performance until fully evaporated.

! **Tighten all SMA connections with 3 in-lb min to 5 in-lb max (56 N-cm max)**

- | | |
|---------------|--|
| LO Out | This port outputs the tunable LO signal allowing phase-coherent daisy-chaining of multiple IQ demodulator modules. The connector is SMA female. The nominal output impedance is 50 Ω . |
| RF In | This port accepts an RF signal ranging from 400 MHz to 6 GHz. The connector is SMA female. The nominal input impedance is 50 Ω . Maximum input power is +23 dBm with ATTEN#1 set to at least 10 dB attenuation. |

RF Aux In	This port accepts an RF signal ranging from 400 MHz to 6 GHz. This port can be used as an alternate path for system-level calibration. The connector is SMA female. The nominal input impedance is 50 Ω .
LO In	This port accepts a tunable LO signal from an external source to drive the demodulator. The connector is SMA female. This port is AC-coupled with a nominal input impedance of 50 Ω . Maximum input power is +10 dBm.

2.3.3 Baseband Connections

The SC5312A and SC5313A have four baseband output ports comprised of differential in-phase (I+ and I-) and differential quadrature (Q+ and Q-) outputs. Nominal differential output impedance is 100 Ω . The demodulator can also be configured for single-ended or differential IF output. When configured for single-ended operation, it is recommended to terminate the other half of the differential pair using a 50 Ω terminator. All baseband connectors are MCX female.

2.3.4 Device LED Indicators

These are two LED indicator lights for the device, and their functions are listed in *Table 1* and *Table 2*.

Table 1. Status LED Indicator (SC5312A ONLY)

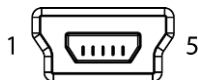
LED Color	Description
Green	The device is functioning properly in the state that it is programmed for.
Off	No supply or supply error.

Table 2. Active LED Indicator (this indicator is user programmable)

LED Color	Description
Green	Device is open. (Communication has been established)
Orange*	Device is powered on and working properly
Off	Device is closed.

*SC5313A ONLY

2.3.5 Mini-USB Connection



The SC5313A uses a mini-USB Type B connector for primary communication with the device using the standard USB 2.0 protocol (full speed) found on most host computers. The pinout of this connector, viewed from the front, is shown in the following table.

PIN #	USB Function	Description
1	VBUS	Vcc (+5 Volts)
2	D-	Serial Data (neg)
3	D+	Serial Data (pos)
4	ID	Not Used
5	GND	Device Ground (also tied to connector shell)

2.3.6 Reset Button (Pin Hole)

Behind this pin hole is the reset button, which is only available on the SC5308A. Using a pin to lightly depress this momentary-action push button switch will cause a hard reset to the device, putting it back to its default settings. All user settings will be lost. System reset capability can also be accessed through the communication header connector.

3 Functional Description

3.1 Overview

The SC5312A uses USB as its primary interface with an optional SPI or RS232 interface. The SC5313A is a PXIe version of the product. They are single-stage, direct conversion Inphase-Quadrature (IQ) demodulating mixers. They can operate as a single-stage downconverter or as an IQ demodulator. These modules operate in the 400 MHz to 6 GHz RF range with a typical 3 dB IF bandwidth of 160 MHz in single-stage converter mode and 320 MHz in IQ mode. The RF input stage has adjustable gain to allow adjustment of the incoming RF signal prior to the demodulation process for the purpose of optimizing RF dynamic range. The IF stage has adjustable gain to ensure that linearity and noise of the IF output are optimized. The modules have the necessary RF amplifiers, attenuators, IF amplifiers, and IF control via DACs to allow the user to optimally operate the device over the entire frequency range as well as for both small and large RF input levels. The following sections provide in depth information on how to optimize the modules for linearity and signal-to-noise dynamic range.

3.1.1 The RF Input

In the design of the RF input section, care was taken to ensure that the dynamic range of the IQ demodulator is preserved as seen at the input port of the device. This requires that the demodulator is not driven too hard (high signal amplitude) or too soft (low signal amplitude). When the device is driven hard, nonlinear effects dominate the system. When driven too softly, signal-to-noise dynamic range suffers. A general rule is to apply more attenuation earlier in the RF signal path to improve linearity, and more gain to improve signal-to-noise performance. As an example, for a given input signal level and while maintaining a relatively constant output IF level, the user would switch in RF AMP#1 and apply attenuation on ATTEN#3 to improve signal-to-noise dynamic range. The factory default state sets all the RF amplifiers off, all attenuators set to 0 dB attenuation, and the IF gain set to 8 dB (DAC code of 32). In this default state, the device is optimized for a -10 dBm RF signal in the 1.0 GHz to 2.4 GHz range. The IF output is typically 0.5 V - 1.0 V peak-to-peak differential at these settings.

The RF amplifiers are used to improve the gain of the device if the input signal is too low or when the losses at higher frequencies are large. RF AMP#1 is usually selected when the RF signals are lower than -25 dBm at the input port. With RF AMP#1 enabled, the device sensitivity is improved and the detection of low level signals is better resolved. RF AMP#2 should be selected and switched into the signal path at RF frequencies greater than 5 GHz, where the signal power loss through the front end prior to the demodulator can be as high as 15 dB due to filter and switch insertion losses. At these high RF frequencies, if the IF gain is at its maximum of 15.75 dB (DAC code = 63) and the IF output level falls below -10 dBm or outside the digitizer's optimal levels, RF AMP#2 should be enabled.

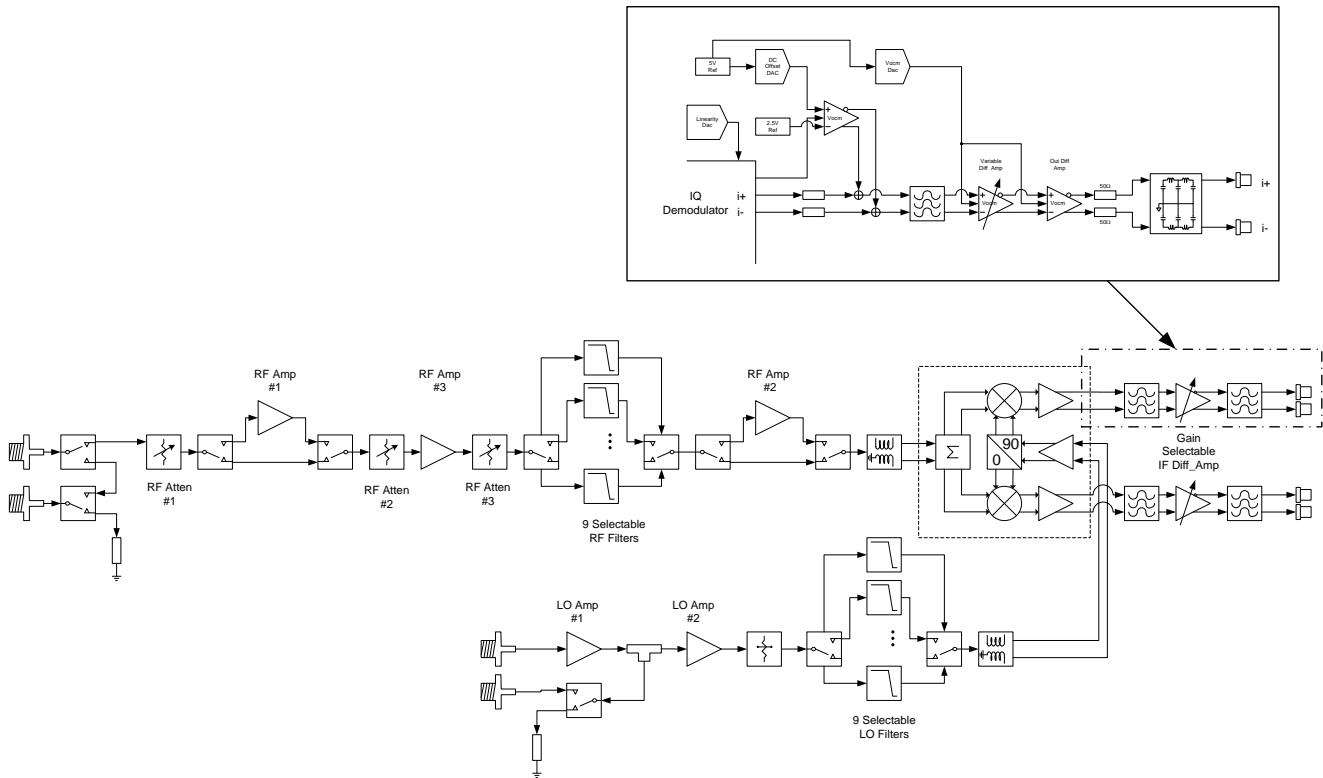


Figure 1. Block diagram of the signal conversion module of the downconverter assembly

The RF attenuators provide attenuation when required. RF ATTEN#1 attenuation should be stepped up as the signal power at the RF port increases above -10 dBm. Nonlinear components of the signal such as IMD3 and second order harmonics will increase in magnitude as the input signal increases; therefore the user should exercise good judgment to determine when to use RF ATTEN#1. Do not over-attenuate. Doing so will negatively impact the signal-to-noise ratio.

RF ATTEN#2 is used when the input signal needs further suppression to improve linearity. It should also be used if RF AMP#1 is enabled to improve sensitivity, but as a result the level at the input of RF AMP#3 (always in the path) may be too high. Step up the attenuation of RF ATTEN#2 to ensure the system (resulting from RF AMP#3) is not driven too hard. Finally RF ATTEN#3 is used to control the level to the IQ demodulator when RF AMP#2 is enabled (switched into the signal path).

There is an auxiliary RF input to the device. This input is almost identical to the main RF input with the exception of having an extra switch path. The intended use of this port is to allow the user a calibration path without having to detach the device under test (DUT) already cabled to the main RF input port. The user must perform in-situ equalization to remove IQ errors such as phase imbalance and quadrature gain offsets that are inherent to the device. Providing this auxiliary path makes the task of characterizing the system with and without a DUT much easier.

There are nine low pass filters in the RF filter bank. These filters are automatically selected when the user enters the operating frequency. These filters can also be selected manually should the user choose to do so. As with all filters there is generally an amplitude roll-off as the frequency nears its 3 dB cutoff point so it is important to understand that frequencies near to the cutoff point may experience a slightly faster roll-off of its IF bandwidth. A typical 1 dB IF bandwidth (IQ) is about 160 MHz. The user may want to choose a higher frequency filter if this becomes a problem. See the programming section in this manual for more details. The filters in both the RF and LO filter banks are identical and are listed below.

Filter Number	1 dB Cutoff Frequency
0	400 MHz
1	500 MHz
2	650 MHz
3	1000 MHz
4	1400 MHz
5	2000 MHz
6	2825 MHz
7	3800 MHz
8	6000 MHz

3.1.2 IF Input Section

The SC5312A and SC5313A require an external RF signal as their “Local Oscillator” (LO) for the frequency conversion process. The external RF signal must be connected to the “LO in” port. The typical required input level is -3 dBm to 3 dBm. These levels are required to sufficiently drive the IQ demodulator for good linearity performance and conversion loss. The LO signal is conditioned through a bank of low-pass filters to reduce the signal harmonics. Reducing the harmonics produces a “purer” signal tone, improving the duty cycle of the LO as it drives the mixers of the demodulator. Additionally, the LO signal can be passed out of the device via the “LO out” port. This output can be used as the input LO source for another demodulator, for example. Driving multiple demodulators with the same derived LO signal optimizes phase coherency between them. When this port is not in use, it is highly recommended to terminate it into a 50 Ω load.

3.1.3 IF Output Section

The IF outputs are differentially driven. Each of the in-phase and quadrature components of the demodulator are conditioned prior to leaving the IF ports. The user can programmatically adjust the parameters of the differential signal such as the common output voltage, DC offset between the (-) and (+) terminals, and its amplitude. The differential output impedance of each component is 100 Ω and DC coupled. However, all ports can be operated as AC coupled single-ended 50 Ω ports. All unused ports should be terminated into AC coupled 50 Ω loads.

There are voltage DACs within the device to control the signal parameters of each of the IQ components. For each component, the Vcom (common voltage) DAC controls the common output voltage of the differential outputs. The Vcom DAC values range from 0 to 16383 (14 bits) and change the voltage between 1 - 3.5 V. For a wider output voltage swing range, this voltage should be set to about 2.4 - 2.5 V. Having a wider swing range improves the output compression point of the device. This is not a hard requirement and the user will need to adjust the voltage levels to suit their specific requirements. As an example, setting to some other voltage may be required to optimize the dynamic range of the receiving digitizer and as a result better optimize the entire system.

DC offsets may limit the dynamic range of the receiving digitizer and where it is critical the user can “tune out” to minimize these offsets using the DC Offset DAC. This 14 bit DAC can correct offsets up to +/-0.050 V with less than 0.010 mV resolution.

The IF amplifiers have adjustable gain ranges from 0 to 15.75 dB, with a tuning resolution of 0.25 dB. The gain is controlled by programming a 6-bit DAC whose codes range from 0 to 63. Writing 63 to the DAC provides the highest gain. Increasing the IF gain instead of the RF gain to achieve a required IF level will improve the linearity of the system but with the chance of a slight increase in output noise. For a common output voltage of 2.4 V, the output compression/saturation point of the amplifier is around 10 dBm. It is recommended to operate the output at least 6 dBm below this value to avoid running into saturation from signals with high crest factors. When deciding the operating point of the digitizer, it is recommended that the user not operate the output voltage too close to the saturation point of the digitizer input.

The linearity DAC controls the current flow through the demodulator core and thus affects the linearity of the device. Generally, increasing the voltage results in higher current consumption, and as a result the linearity improves. However slight adjustments to the voltage may improve the linearity further; this is dependent on the frequency and input power.

4 Hardware Registers

The set of hardware registers of the downconverter may be divided into a configuration set and a query set; the configuration registers are write-only registers to set up the states of the device, while the query registers request the device to prepare and send back data associated with them. The registers are identical for all communication interfaces: PXIe, USB, RS232, and SPI. Data communication to all interfaces are sent in 1 byte wide, that is, data is transferred byte-by-byte. Register data lengths vary in size, and it is important that the correct number of bytes are sent for the corresponding register. Failure to do so may cause communication to lock-up and the device to become unresponsive.

4.1 Configuration Registers

These are write-only registers to configure the device. The registers vary in length to reduce redundant data and improve the communication speed, especially for SPI and RS232 interfaces. Furthermore, it is vitally important that the length of data written to a register is exact because failure to do so will cause the interfaces to misinterpret the incoming data, leaving the device in a stalled state. The total number of bytes is the sum of the register address (1 Byte) and its corresponding data bytes. For example, to set the RF frequency value, eight bytes must be written; the sum of the 1 register byte and 7 data bytes. See the RF_FREQUENCY register of Table 3. The table provides a summary of the configuration registers, and each register is explained in detail.

Table 3. Configuration Registers

Register Name	Reg Add	Serial Range	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
INITIALIZE	0x01	[7:0]	Set to zeros [7:1]								Mode
SYSTEM_ACTIVE	0x02	[7:0]	Set to zeros [7:1]								Enable "active" LED
SYNTH_MODE	0x03	[7:0]	Set to zeros [7:2]						Fast-tune	Loop Gain	
RF_FREQUENCY	0x10	[7:0]	Frequency Word (Hz) [7:0]								
		[15:8]	Frequency Word (Hz) [15:8]								
		[23:16]	Frequency Word (Hz) [23:16]								
		[31:24]	Frequency Word (Hz) [31:24]								
		[39:32]	Frequency Word (Hz) [39:32]								
		[47:40]	Frequency Word (Hz) [47:40]								
		[55:48]	Set to zeros								LO
IF_FREQUENCY	0x11	[7:0]	Frequency Word (Hz) [7:0]								
		[15:8]	Frequency Word (Hz) [15:8]								
		[23:16]	Frequency Word (Hz) [23:16]								
		[31:24]	Frequency Word (Hz) [31:24]								
		[39:32]	Frequency Word (Hz) [39:32]								
		[47:40]	Frequency Word (Hz) [47:40]								
		[55:48]	Set to zeros								
RF_AMP	0x14	[7:0]	Set to zeros [7:1]								Enable
ATTENUATOR	0x15	[7:0]	0	Attenuator value							
		[15:8]	Set to zeros [15:11]					Attenuator Number			
		[23:16]	Set to zeros [23:16]								
SIGNAL_PATH	0x16	[7:0]	If3 fil#2 select	If3 fil#1 select		If2 filter select	0	Bypass IF3 conv	Ext. IF2 select	Bypass convert	
		[15:8]	Set to zeros [15:10]						Rf amp	invert	

Register Name	Reg Add	Serial Range	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		[23:16]	Set to zeros [23:16]							
CONFIG_AUTO_GAIN	0x17	[7:0]	Set to zeros [7:5]			Linear mode		Auto ctrl amp	Load params	Auto Enable
		[15:8]	Sign	Absolute RF level (0 - 127) dB [6:0]						
		[23:16]	Sign	Absolute mixer level (0 - 127) dB [6:0]						
		[31:24]	Sign	Absolute IF level (0 - 127) dB [6:0]						
		[39:32]	Set to zeros							
STORE_DEFAULT_STATE	0x18	[7:0]	Set all to zeros							
DEVICE_STANDBY	0x19	[7:0]	Set to zeros [7:4]				Device sections			Enable
REFERENCE_CLOCK	0x1A	[7:0]	[7:4] set to zeros			PXI 10 enable	Clk 100 enable	Ref out enable	Lock ext	
REFERENCE_DAC	0x1B	[7:0]	DAC WORD [7:0]							
		[15:8]	0	0	DAC WORD [13:8]					
		[23:16]	Set to zeros							
LO1_PATH	0x1C	[7:0]	0	0	0	0	0	0	0	Ext/Int
SYNTH_SELF_CAL	0x1D	[7:0]	Set all to zeros							
USER_EEPROM_WRITE	0x1E	[7:0]	BYTE DATA [7:0]							
		[15:8]	ADDRESS [7:0]							
		[23:16]	ADDRESS [15:8]							
FREQ_PLAN_PARAM	0x1F	[7:0]	Frequency word (Hz) [7:0]							
		[15:8]	Frequency word (Hz) [15:8]							
		[23:16]	Frequency word (Hz) [23:16]							
		[31:24]	Frequency word (Hz) [31:24]							
		[39:32]	Frequency word (Hz) [39:32]							
		[47:40]	Frequency word (Hz) [47:40]							
		[55:48]	Set to zeros [55:52]				PARAM [3:0]			

4.1.1 Register 0x02 SET_SYS_ACTIVE

This register turns on or off the active LED indicator on the front connector interface of the device. This register should be called when the device is opened or closed in software.

Bytes written | 2
Bytes read | 1

Bits	Type	Name	Width	Description
[0]	WO	Mode	1	0 = Turns off the active LED 1 = Turns on the active LED
[7:1]	WO	Unused	7	Set to zeros
[7:0]	RO	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.2 Register 0x03 SYNTH_MODE (2 Bytes)

This register configures the PLL loop gain of the local oscillator synthesizers. It also enables or disables faster tuning of the YIG based oscillator of LO1.

Bytes written | 2
Bytes read | 1

Bits	Type	Name	Width	Description
[1:0]	WO	Loop Gain	2	0 = Low loop gain, improves phase noise > 50 kHz 1 = Normal loop gain 2 = High loop gain, improves phase noise < 50 kHz
[2]	WO	Fast Tune	1	0 = Turns fast tune off, default 1 = Turns fast tune on, close in phase noise may degrade
[7:3]	WO	Unused	5	Set to zeros
[7:0]	RO	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.3 Register 0x10 RF_FREQUENCY

This register tunes the device to the input RF frequency.

Bytes written | 8
Bytes read | 1

Bits	Type	Name	Width	Description
[47:0]	W	Frequency word	48	Frequency word in milli-Hz (mHz); mHz used for future compatibility
[48]		LO	1	Set to 1 to apply value directly to the first LO. The RF frequency value is unchanged.
[55:49]	W	Unused	7	Set to zeros
[7:0]	RO	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.4 Register 0x11 IF_FREQUENCY

This register sets the final IF value.

Bytes written | 2
Bytes read | 1

Bits	Type	Name	Width	Description
[47:0]	W	Frequency word	48	Frequency word in milli-Hz (mHz); mHz used for future compatibility
[55:48]	W	Used	8	Set to zeros
[7:0]	R	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.5 Register 0x14 RF_AMP

This register enables and disables the RF amplifier.

Bytes written | 2
Bytes read | 1

Bits	Type	Name	Width	Description
[0]	W	Frequency word	1	0 = Disables the RF amplifier 1 = Enables the RF amplifier
[7:1]	W	Unused	7	Set to zeros
[7:0]	R	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.6 Register 0x15 ATTENUATOR

This register sets the value of the device attenuators.

Bytes written | 4
Bytes read | 1

Bits	Type	Name	Width	Description
[7:0]	W	Attenuator value	8	In 0.25 dB steps, i.e. LSB = 0.25 dB

Bits	Type	Name	Width	Description
[10:8]	W	The target attenuator	3	The attenuator number: 0 = RF Atten #1 1 = RF Atten #2 2 = not used 3 = External IF input IF2 Atten 4 = IF3 Atten #1 5 = IF3 Atten #2
[23:11]	W	Unused	13	Set to zeros
[7:0]	R	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.7 Register 0x16 SIGNAL_PATH

This register configures how the signal chain is routed.

Bytes written		2
Bytes read		1

Bits	Type	Name	Width	Description
[0]	W	bypassConverter	1	0 = Normal conversion path 1 = Bypasses the conversion, switches RF input directly to IF3 output
[1]	W	If2ExtSelect	1	0 = Deselects 1 = Selects the IF2 input port
[2]	W	bypassIF3Conv	1	0 = IF2 is converted to IF3 1 = IF2 is switched to IF3 output port, bypassing mixer 3 conversion
[3]	W	If1Filter	1	Not implemented
[4]	W	IF2Filter	1	0 = Selects the 160 MHz IF2 filter 1 = Selects the 80 MHz IF2 filter
[6:5]	W	IF3Filter1	2	First filter bank of IF3: 0 = Selects the 500 MHz LPF 1 = Selects the 250 MHz LPF 2 = Selects a through path 3 = Not implemented

Bits	Type	Name	Width	Description
[7]	W	If3Filter2	1	Second filter bank of IF3: 0 = 1500 MHz LPF, this should always be selected when IF3 conversion is enabled 1 = A narrow 1.25 GHz bandpass filter
[8]	W	invertSpectrum	1	0 = Not spectral inversion 1 = IF3 spectrum inverted w.r.t RF
[9]	W	rfAmp	1	0 = Disables RF amp 1 = Enables RF amp
[23:10]	W	Not used	14	Set to zeros
[7:0]	R	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.8 Register 0x17 CONFIG_AUTO_GAIN

This register will configure the device to set the attenuator values and control the RF amplifier to keep the device gain close to the desired gain with changes in RF frequency, as computed from its input parameters such as RF input level, mixer level, and IF out level.

Bytes written		6
Bytes read		1

Bits	Type	Name	Width	Description
[0]	W	autoGainEnable	1	0 = Attenuator and RF amplifier states are not manipulated when RF values are changed 1 = Computes and applies new sets of attenuator and amplifier states to the device as frequency is changed
[1]	W	loadParams	1	0 = Not to load new input parameter such as RF level, etc. Will not load any information from bits [47:2] 1 = Will load bits [31:2]
[2]	W	autoCntrlRfAmp	1	0 = Computation will leave the state of the RF amplifier unchanged 1 = Computation will change the state of the RF amplifier to provide the best device configuration to meet the input parameter requirements

Bits	Type	Name	Width	Description
[4:3]	W	linearMode	2	0 = Best signal-to-noise (SNR), least linear 1 = Better SNR, sufficiently linear 2 = Better linearity, sufficient SNR 3 = Best linearity, least SNR
[7:5]	W	Unused	3	Set to zeros
[14:8]	W	rfLevel	7	Set the absolute level of the expected RF input level in dB.
[15]	W	rfLevel Sign bit	1	0 = Positive 1 = Negative
[22:16]	W	mixerLevel	7	Set the absolute level of the expected input mixer level in dB
[23]	W	mixerLevel Sign bit	1	0 = Positive 1 = Negative
[30:24]	W	ifLevel	7	Set the absolute level of the expected output IF3 level in dB
[31]	W	ifLevel Sign bit	1	0 = Positive 1 = Negative
[39:32]	W	Unused	8	Set to zeros
[7:0]	R	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.9 Register 0x18 STORE_DEFAULT_STATE

This register will store all current settings of the device into EEPROM and will become the default startup setting.

Bytes written		2
Bytes read		1

Bits	Type	Name	Width	Description
[7:0]	W	Unused	8	Set to zeros
[7:0]	R	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.10 Register 0x19 DEVICE_STANDBY

This register sets either the entire device or sections of the device into standby mode. Placing a section into standby involves powering down its circuitry. This conserves power and eliminates unwanted LO signals when they are not used.

Bytes written | 2
Bytes read | 1

Bits	Type	Name	Width	Description
[0]	W	State	1	0 = Active 1 = Standby enabled
[3:1]	W	Section	3	0 = Entire device 1 = LO1 2 = LO2 3 = LO3 4 = Signalchain
[7:4]	W	Unused	4	Set to zeros
[7:0]	R	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.11 Register 0x1A REFERENCE_CLOCK

This register configures the reference clock behavior.

Bytes written | 2
Bytes read | 1

Bits	Type	Name	Width	Description
[0]	W	LockEnable	1	0 = Uses internal 10 MHz TCXO 1 = Enables frequency locking to external 10 MHz reference source
[1]	W	RefOutEnable	1	Reference out port enabled
[2]	W	Clk10Enable	1	0 = 10 MHz output 1 = 100 MHz output
[3]	W	PXI10Enable	1	Only on SC5307A to enable export of the 10 MHz backplane clock

Bits	Type	Name	Width	Description
[7:2]	W	Unused	4	Set to zeros
[7:0]	R	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.12 Register 0x1B REFERENCE_DAC

This register makes adjustments to the 10 MHz TCXO accuracy via DAC to its tuning port.

Bytes written | 4
Bytes read | 1

Bits	Type	Name	Width	Description
[15:0]	W	Tuning DAC word	16	DAC WORD
[23:16]	W	Unused	8	Set to zeros
[7:0]	R	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.13 Register 0x1C LO1_PATH

This register sets the path of LO1; either it drives the internal IF1 mixer, or drives out to the LO OUT port connector.

Bytes written | 2
Bytes read | 1

Bits	Type	Name	Width	Description
[0]	W	Path	1	0 = LO1 drives IF1 Mixer 1 = Drives LO1 to LO OUT port
[7:1]	W	Unused	7	Set to zeros
[7:0]	R	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.14 Register 0x1D SYNTH_SELF_CAL

This register will start the YIG synthesizer calibration. Note that although the calibration procedure takes about 6-8 seconds to complete, the register returns a byte almost immediately.

Bytes written | 2

Bytes read | 1

Bits	Type	Name	Width	Description
[7:0]	W	Unused	8	Set to zeros
[7:0]	R	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.15 Register 0x1E USER_EEPROM_WRITE

This register writes a byte to the onboard EEPROM.

Bytes written | 2
Bytes read | 1

Bits	Type	Name	Width	Description
[7:0]	W	Data	8	Byte to be written to the address
[23:8]	W	Address	16	EEPROM address
[7:0]	R	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.1.16 Register 0x1F FREQ_PLAN_PARAM

This register sets up the frequency plan parameters and stores them as the default values.

Bytes written | 8
Bytes read | 1

Bits	Type	Name	Width	Description
[47:0]	W	Data	48	Data for the parameter
[50:48]	W	Parameter	3	0 = RF frequency 1 = IF1 frequency 2 = IF2 frequency 3 = IF3 frequency
[55:51]	W	Unused	5	Set to zeros
[7:0]	R	Read back byte	8	Read 1 byte back is required for PXIe and RS232

4.2 Query Registers

These are request for data registers, in that a request for certain data is made by writing to the specific register first, followed by reading back the requested data. Some registers may require instruction data to specify the type of data to return, while others do not need any. For example, the register GET_DEVICE_PARAM (0x30) returns the RF Frequency, IF1 Frequency, IF3 Frequency, etc.; the data returned depends on the parameter value of the instruction byte.

Returned data length is always 8 bytes (64 bits), with the first byte being the most significant (MSB). It is **important that all 8 bytes** are read to clear the interface buffers. How the different interface buses handle the return data is explained in the *Device Information Parameters and Format* section.

Table 4. Query Registers

Register Name	Reg Add	Serial Range	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GET_DEVICE_PARAM	0x30	[7:0]								Parameter
GET_TEMPERATURE	0x31	[7:0]	Zeros [7:0]							
GET_DEVICE_STATUS	0x32	[7:0]	Zeros [7:0]							
GET_DEVICE_INFO	0x33	[7:0]								Info
CAL_EEPROM_READ	0x34	[7:0]	EEPROM ADDRESS [7:0]							
		[15:8]	EEPROM ADDRESS [15:8]							
USER_EEPROM_READ	0x35	[7:0]	EEPROM ADDRESS [7:0]							
		[15:8]	EEPROM ADDRESS [15:8]							
SERIAL_OUT_BUFFER	0x36	[7:0]	Zeros [7:0]							
		[15:8]	Zeros [15:8]							
		[23:16]	Zeros [23:16]							
		[31:24]	Zeros [31:24]							
		[39:32]	Zeros [39:32]							
		[47:40]	Zeros [47:40]							
		[55:48]	Zeros [55:48]							

4.2.1 Register 0x30 GET_DEVICE_PARAM

Write to this register the required device parameter to query from the device.

Bytes written		2
Bytes read		8

Bits	Type	Name	Width	Description
[3:0]	W	Parameter	1	0: Returns current RF frequency 1: Current IF1 frequency 2: Current IF2 frequency 3: Current IF3 frequency 4: Current LO1 frequency 5: Current LO2 frequency 6: Current LO3 frequency 7: Current attenuator values 8: Current signalchain configuration
[7:4]	W	Unused	4	Set to zeros
[63:0]	R	Read back bytes	64	Returned Data (See Device Parameter Data section for more info)

4.2.2 Register 0x31 GET_TEMPERATURE

Write to this register to query the device temperature.

Bytes written		2
Bytes read		8

Bits	Type	Name	Width	Description
[7:0]	W	Unused	7	Set to zeros
[31:0]	R	Temperature Data	32	These 32 bits of data need to be type casted back to float. i.e. var_float = *(float*)&var_u32 where var_u32 is some unsigned integer that holds the 32 bits of read data.
[63:32]	R	Invalid data	32	Ignore

4.2.3 Register 0x32 GET_DEVICE_STATUS

Write to this register to query the current operating conditions.

Bytes written		2
Bytes read		8

Bits	Type	Name	Width	Description
[7:0]	W	Unused	7	Set to zeros
[0]	R	PLL status: LO1 sum	1	The summing PLL of LO1
[1]	R	PLL status: LO1 crs	1	The coarse tuning PLL of LO1
[2]	R	PLL status: LO1 fine	1	The fine tuning PLL of LO1
[3]	R	PLL status: LO2	1	LO2
[4]	R	PLL Status: LO3	1	LO3
[5]	R	PLL status: VCXO	1	100 MHz OCXO
[6]	R	PLL status: TCXO	1	TCXO, only valid when lock to external reference is enabled
[7]	R	PLL status: ref_detect	1	Detected a reference signal of sufficient amplitude
[8]	R	Device Accessed	1	When the SET SYS ACTIVE register is accessed
[9]	R	LockExtRef	1	Enable device to lock to external reference
[10]	R	RefOutEnable	1	Reference output enable
[11]	R	RefOutFreqSelect	1	10MHz(0) or 100MHz(1) selected as output reference frequency
[12]	R	Lo1PwrUp	1	LO1 synth power up
[13]	R	Lo2PwrUp	1	LO2 synth power up
[14]	R	Lo3PwrUp	1	LO3 synth power up
[16:15]	R	loopGain	2	Loop gain of the Synthesizers
[17]	R	fastTune	1	LO1 set to fast tune
[18]	R	Lo1OutEnable	1	LO1 route to output port
[23:19]	R	Reserved	2	Invalid

Bits	Type	Name	Width	Description
[24]	R	scPwrUp	1	Signalchain power up
[25]	R	bypassConv	1	RF conversion bypassed, direct to IF3
[26]	R	If2ExtSelect	1	IF2 input from external port select
[27]	R	bypassIF3Conv	1	IF3 conversion bypassed, IF2 directed to IF3 output port
[28]	R	Reserved	1	Ignore
[29]	R	IF2FilterSelect	1	IF2 filters: 0 = 160 MHz, 1 = 80 MHz
[31:30]	R	IF3Filter1Select	2	IF3 filter bank #1 filter select
[32]	R	IF3Filter2Select	1	IF3 filter bank #2 select
[33]	R	invertSpectrum	1	RF amplifier enable
[34]	R	rfAmpEnable	1	Spectrum at IF3 is inverted
[35]	R	autoGainEnable	1	Auto calculation of gain enabled (default 0). Software gain calculation used.
[36]	R	autoRfAmp	1	Auto set the RF preamplifier when autoGainEnable = 1
[37]	R	Reserved	1	n/a
[63:38]	R	Invalid data	29	Ignore

4.2.4 Register 0x33 GET_DEVICE_INFO

Write to this register to query the device information such as serial number.

Bytes written		2
Bytes read		8

Bits	Type	Name	Width	Description
[3:0]	W	DeviceInfo	4	0: Product serial number and Interface type 1: Firmware and hardware revision 2: Calibration and manufacture date 3: Device interface 4: Manufacture date 5: Last calibration date
[7:4]	W	Unused	4	Ignore
[63:0]	R	Data	64	Information data (see Device Info data)

4.2.5 Register 0x34 CAL_EEPROM_READ

Write to this register to query 8 bytes of data from the user EEPROM at the starting address.

Bytes written		4
Bytes read		8

Bits	Type	Name	Width	Description
[15:0]	W	Address	16	Starting EEPROM address
[23:16]	W	Unused	8	Zeros
[63:0]	R	Data	64	8 bytes of data, LSB is the byte at the start address

4.2.6 Register 0x35 USER_EEPROM_READ

Write to this register to query 8 bytes of data from the user EEPROM at the starting address.

Bytes written		4
Bytes read		8

Bits	Type	Name	Width	Description
[15:0]	W	Address	16	Starting EEPROM address
[23:16]	W	Unused	8	Zeros
[63:0]	R	Data	64	8 bytes of data, LSB is the byte at the start address

4.2.7 Register 0x36 SERIAL_OUT_BUFFER

Writing to this register only provides the 64 clock edges (Reg + 7 data bytes) to transfer serial data from the device through SPI. Other interfaces do not use this register.

Bytes read | 8

Bits	Type	Name	Width	Description
[55:0]	W	Unused	56	Zeros, just to provide clocking for SPI data from device
[63:0]	R	Data	64	8 bytes of data

4.2.8 Device Parameters Data and Format

The data read back from the GET_DEVICE_PARAM register has a total of 8 bytes, however not all bytes contain valid data. The table below shows the valid data for each of the parameters.

Table 5. Device parameter data

Device Parameter Name	Param num	Data type	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
RF FREQ	0	U64	zeros	Data						
IF1 FREQ	1	U64	zeros	Data						
IF2 FREQ	2	U64	zeros	Data						
IF3 FREQ	3	U64	zeros	Data						
LO1 FREQ	4	U64	zeros	Data						
LO2 FREQ	5	U64	zeros	Data						
LO3 FREQ	6	U64	zeros	Data						
ATTEN VALUES	7	8xU8	zeros	NA	RF A1	RF A2	NA	EXT IF	IF3 A1	IF3 A2
CHAIN CONFIG	8	2xU16	zeros	zeros	zeros	zeros	SC Gain		SC Config	

4.2.8.1 Frequency parameter values

Frequency parameter values are returned in the first 7 bytes with the last byte padded with zeros. The least significant bit (LSB) is 1/1000 Hertz (the data is returned in 1 one thousandth of a Hertz). Divide the data by 1000 to obtain the result in Hertz.

4.2.8.2 Attenuator values

Each attenuator value is returned as one byte, and the LSB is in 0.25 dB. Divide each byte by 4 to obtain the result in dB.

4.2.8.3 Signal Chain Configuration

The signal chain configuration data is in the first 2 bytes, and their data is represented in the following table.

Table 6. Signal chain configuration data representation

Bit	Description
[0]	Bypass Conversion
[1]	IF2 external port select
[2]	Bypass IF3 conversion
[3]	NA
[4]	IF2 filter selection 0 = 160 MHz, 1 = 80 MHz
[6:5]	IF3 Filter 1 selection
[7]	IF3 Filter 2 selection
[8]	IF spectral inversion
[9]	RF preamplifier state

The first order computed gain (device approx.) of the device is returned in bytes 3 and 4. Data bits [14:0] represent the absolute value in 1/100 of a dB, while bit [15] is the sign bit.

4.2.9 Device Information Parameters and Format

Not all the 8 bytes read back contain valid data. The following table shows the valid bytes of data for each of the parameters.

Device Parameter Name	Param num	Data type	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
INTERFACE	0	U32				Intrfce	Serial Number			
REVISIONS	1	F32	Software revision				Firmware revision			
DATES	2	U32	Cal year	Month	Day	Mfg year	Month	Day		

4.2.9.1 Interface Information

The first 4 bytes contain the device serial number as an unsigned 32-bit integer. Byte [4] contains the interface as represented in the following table.

Table 7. Interface ID

Bit	Description
[0]	PXI/PXIe (1 if available)
[1]	USB

[2]	SPI
[3]	RS232
[7:4]	Undefined

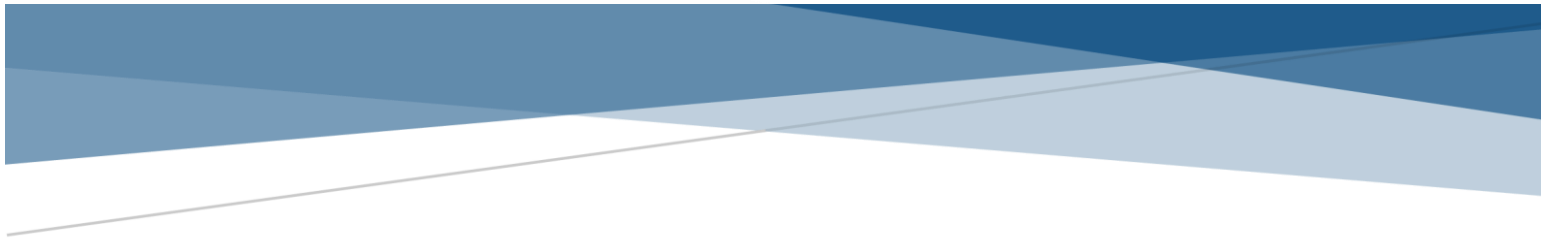
4.2.9.2 Revision Information

The first 4 bytes represent the hardware revision and the last 4 bytes represent the firmware revision of the device. These 4 bytes encompass a 32-bit floating point number so the data needs to be type casted from an unsigned 32-bit value to float value.

4.2.9.3 Date Information

The first 4 bytes represent the manufactured date and the last 4 bytes represent the last calibration date. The date format is outlined in the following table.

Bit	Type	Description
[0]	U8	Day
[1]	U8	Month
[4:3]	U16	Year (i.e. 2016)



Section 2

Communication Interfaces and Calibration

5 Communication Interfaces

The SC5307A has a PXI express interface, while the SC5308A has 2 communication interfaces:

1. USB and SPI
2. USB and RS232

This section will examine the communication aspects of the product, focusing on data transfer to and from the device on each interface. Although the registers are identical for all interfaces, there are subtle differences in the implementation of the interfaces to transfer the data.

5.1 Communication Data Format

All data sent and received by all interfaces is sent as buffers of unsigned bytes. For example, to change RF frequency of the device to 6 GHz we perform the following:

1. Frequency is sent in 1000th of Hertz, so the data that represents the frequency is 6,000,000,000,000 milli-Hertz.
2. This number can be represented by a 64-bit unsigned long, and in Hexadecimal is 0x 0000 0574 FBDE 6000. Only the least 6 bytes are needed to represent all frequencies allowable for this device.
3. A byte data buffer needs to be 8 bytes for register RF_FREQUENCY (address 0x10), so the byte array buffer to be sent would be:

```
[0x10][0x00][0x05][0x74][0xFB][0xDE][0x60][0x00]
```

The register address byte [0x10] is the first member of the buffer to be sent.

5.2 USB Interface

There are 2 transfer types for the USB interface.

- Control transfer
- Bulk transfer

5.2.1 Control Transfer

The USB control transfer parameters are:

ENDPOINT_IN	0x80
ENDPOINT_OUT	0x00
TYPE_VENDOR	0x40
RECIP_INTERFACE	0x01

5.2.2 Bulk Transfer

The USB bulk transfer parameters are:

ENDPOINT_IN	0x83
ENDPOINT_OUT	0x04

The bulk transfer from the host to the device operates on a loopback with a data buffer of 8 bytes. When a device register is addressed, and upon completion of the register task, such as changing frequency, it will send back 8 bytes, which the host must read to clear the transfer buffers. Unlike the other interface methods, where only the required number of bytes needs to be sent for a given register, 8 bytes are needed for every USB bulk transfer. For example, if a configuration register requires only 4 bytes to be sent, these bytes will be the first of the 8 bytes and the last 4 bytes are zeros. The returned 8 bytes do not carry valid data for a configuration register. However, they do carry valid data for query registers.

5.3 SPI Interface

The SPI interface on the device is implemented using an 8-bit (single Byte) buffer for both the input and output, hence, it needs to be read and cleared by the device before consecutive bytes can be transferred to and from it. The process of clearing the SPI buffer and decisively moving it into the appropriate register takes CPU time, so a time delay is required between consecutive bytes written to or read from the device by the host. The chip-select pin (\overline{CS}) must be asserted low before data is clocked in or out of the product. Furthermore, pin \overline{CS} must be asserted low for the entire duration of a register transfer.

Once a full transfer has been received, the device will proceed to process the command and de-assert low the SRDY pin. The status of this pin may be monitored by the host because when it is de-asserted low, the device will ignore any incoming data. The device SPI is ready when the previous command is fully processed and the SRDY pin is re-asserted high. It is important that the host either monitors the SRDY pin or waits for 500 μs between register writes.

There are 2 SPI modes: 0 and 1. The default mode is 1, where data is clocked in and out of the device on the falling edge of the clock signal. In mode 0, data is clocked in and out on the rising edge. To select mode 0, pin 23 of the interface connector must be pulled low to ground as the device is powered on or as the reset line (pin 19) is toggled low-high. If pin 23 is pulled high or left unconnected, mode 1 is selected.

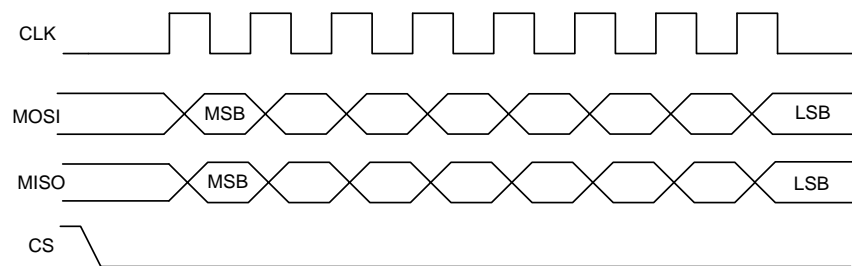


Figure 2. SPI Mode 1 shown.

Register writes are accomplished in a single write operation. Register lengths vary depending on the register. They vary in lengths of 2 to 8 bytes, with the first byte sent being the register address followed by the data associated with that register. The (\overline{CS}) pin must be asserted low for a minimum period of 1 μs (T_S , see Figure 3) before data is clocked in, and must remain low for the entire register write. The clock rate may be as high as 5.0 MHz ($T_C = 0.2 \mu\text{s}$), however, if the external SPI signals do not have sufficient integrity due to trace issues, the rate should be lowered.

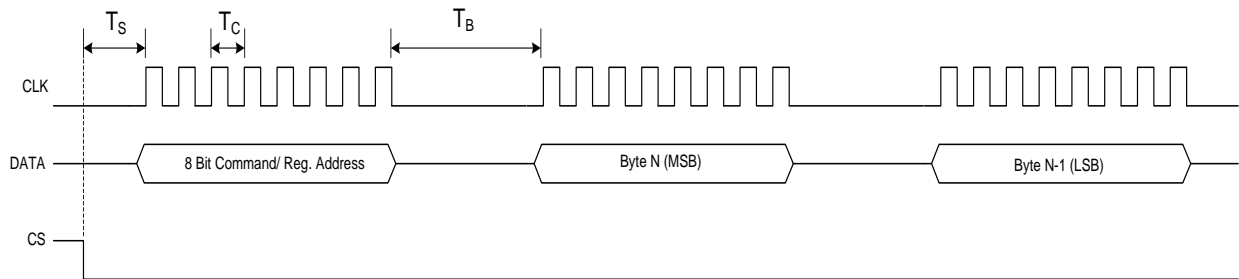


Figure 3. SPI timing.

As mentioned above, the SPI architecture limits the byte rate since after every byte transfer the input and output SPI buffers need to be cleared and loaded respectively by the device SPI engine. Data is transferred between the input buffer and internal register buffers. The time required to perform this task is indicated by T_B , which is the time interval between the end of one byte transfer and the beginning of another. The recommended minimum time delay for T_B is 1 μs . The number of bytes transferred depends on the register. It is important that the correct number of bytes is transferred for the associated register, because once the first byte (MSB) containing the device register address is received, the device will wait for the desired number of associated data bytes. The device will hang if an insufficient number of bytes are written to the register. To clear a hung condition, the device will need an external hard reset. The time required to process a command is also dependent on the command itself. Measured times for command completions are typically between 50 μs to 300 μs after reception.

5.3.1 Writing the SPI Bus

The SPI transfer size (in bytes) depends on the register being targeted. The first byte sent is the register address and subsequent bytes contain the data associated with the register. As data from the host is being transferred to the device via the MOSI line, data present on its SPI output buffer is simultaneously transferred back, MSB first, via the MISO line. The data returned is invalid for configuration registers. The following figure shows the contents of a single 3-byte SPI command written to the device. The Hardware Registers section provides information on the number of data bytes and their contents for an associated register. There is a minimum of 1 data byte for each register even if the data contents are “zeros”.

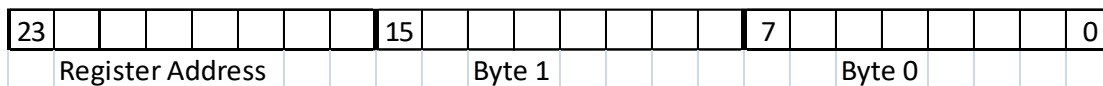


Figure 4. Example of a 3-byte write

5.3.2 Reading the SPI Bus

Data is simultaneously read back during an SPI transfer cycle. Requested data from a prior command is available on the device SPI output buffers, and these are transferred back to the user host via the MISO pin. To obtain valid requested data would require querying the SERIAL_OUT_BUFFER, which requires 8 bytes or 64 clock cycles; 1 byte for the device register (0x37) and 7 empty bytes (MOSI) to clock out the returned data (MISO). An example of reading the device RF parameters (IF3 frequency) from the device is shown in the following figure.

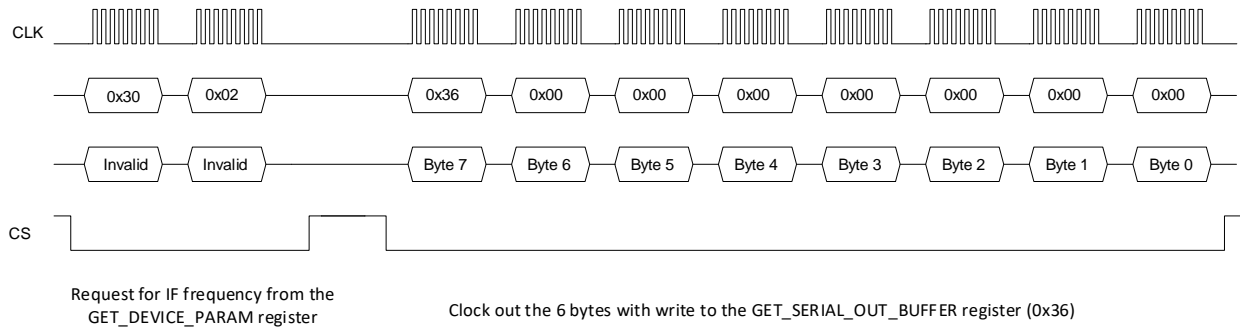


Figure 5. Query example: Write followed by Read to the GET_SERIAL_BUFFER

In the figure above, the first transfer cycle is to make the request for IF3 frequency data through the GET_DEVICE_PARAM register. The subsequent cycle is to clock the data that was requested by sending 64 clocks into the GET_SERIAL_BUFFER register.

5.4 RS232 Interface

The RS232 version of the SC5308A has a standard interface buffered by an RS232 transceiver so that it may interface directly with many host devices, such as a desktop computer. The interface connector for RS232 communication is labeled “Digital I/O” on the front of the panel. Refer to *Error! Reference source not found.* for position and pin-out information. The RS232 device communication control set is provided in the following table.

Table 8. RS232 Control Setting

Baud rate	Rate of transmission *Pin 16 of the Digital IO connector selects the rate. By default, if the pin is pulled high or open, the rate is set to 56700 at power up or upon HW reset. When the pin is pulled low or grounded, the rate is set to 115200 upon reset or power up.
Data bits	The number of bits in the data is fixed at 8.
Parity	Parity is 0 (zero)
Stop bits	1 stop bit
Flow control	0 (zero) or none

Only 3-wire RS232 is required since hardware flow control is not used. These connections are the Tx, Rx, and Gnd. This interface is common on most host computers and microcontrollers, so user access to host ports is readily provided by the computer OS or microcontroller hardware registers.

5.4.1 Writing to the Device Via RS232

It is important that all necessary bytes associated with any one register are fully sent. In other words, if a register requires a total of 6 bytes (address plus data), then all 6 bytes must be sent even though the last byte may be null. The device, upon receiving the first register addressing byte, will wait for all the associated data bytes before acting on the register instruction. Failure to complete the register

transmission will cause the device to behave erratically or hang. Information for writing to the configuration registers is provided in *Table 3. Configuration Registers*. Upon the execution of the register that was sent, the device will return one (1) byte of data with bit 1 high to indicate success. This byte must be read by the host to clear its receive buffer so that reading subsequent registers will not contain corrupted data. Furthermore, reading back this byte will ensure that the device is ready for the next register command.

5.4.2 Reading from the Device Via RS232

To query information from the device, the query registers are addressed, and data is returned. *Table 4. Query Registers* contains the query register information. As with the configuration registers, it is important that all data byte(s) (write) associated with the query registers are sent even if they are null. All queries will return 8 bytes of data (read) with the first received byte being the most significant (MSB). Section 4.2 *Query Registers* provides the format details of the received data.

5.5 PXI Express

The PXIe interface contains a high-speed PCIe-to-Serial bridge chip. This bridge chip communicates with the onboard microcontroller serially. The interface on the bridge chip resides at offset addresses between 0x00 and 0xFF from BAR0; which is memory mapped. A kernel level driver for the operating system is needed to access this memory address. A simple driver using IO controls should be sufficient to read and write byte data to this block of addresses. Although SignalCore provides the driver and API for these products, information is provided here for users who may need to write drivers for a different operating system or a different driver. An example would be writing the API for the Linux operating system.

5.5.1 Setting Up the PCI to Serial Bridge

The serial function of the bridge chip must first be initialized before it can communicate with the onboard microcontroller, and hence communication between the microcontroller and the PXIe bus. The initialization can be done at the kernel level mode or at the user level mode, the decision is left to the user. The following table lists the programming order of the bridge register addresses to initialize and setup the serial port function.

Step	BAR0 Register Address	Data (Byte)
1	0x10CC	0x00
2	0x1004	0x80
3	0x10C2	0x04
4	0x10C1	0x00
5	0x10C3	0x01
6	0x1003	0x80
7	0x1000	0x10
8	0x1001	0x00
9	0x1003	0x03
10	0x1002	0x07

5.5.2 Writing to the Device

Bytes that are written to the device must go through the bridge chip. In this section, we will first look at the write cycle of each byte, and then the write cycle of each device register. Do note the difference between the bridge register addresses and the device register addresses.

5.5.2.1 Single Byte Write

The serial transfer buffer register address is located at 0x1000 offset from BAR0 of the bridge chip, however, before writing byte data to this register, its status needs to be checked to confirm that it is ready to accept a new buffer set of bytes. The status register is located at 0x1005; it must be read and bit 7 must be **high** to indicate that the transfer register is ready to receive the next byte buffer. Checking the status register of the serial bridge chip is required before every new command write.

5.5.2.2 Device Register Write

The process of writing the device registers is the same as writing an RS232 port, so the description of Section 5.4.1 *Writing to the Device Via RS232* is applicable. Writing the device registers involves sending byte-by-byte data as described previously. Section 4.1 *Configuration Registers* provides information on the number of configuration write bytes needed for each device register. The first byte sent is the device register address, followed by the most significant byte of the register's associated data. When a device register is fully written, that is, all its data has been sent to the device, it will return 1 byte. This returned byte must be read (by the host) to clear the transfer buffer so that later received data are not corrupted. Section 5.5.3.1 *Single Byte Read* describes how a byte read cycle is performed.

5.5.3 Reading from the Device

Device data is passed back to the host via the bridge chip byte-by-byte. Details about a single byte read process and an entire register read process are explained in the following subsections.

5.5.3.1 Single Byte Read

The serial transfer buffer register address is located at 0x00 offset from BAR0 of the bridge chip. Before valid data can be read from the transfer register, its ready status must first be confirmed. The status register is located at 0x05; it must be read and bit 0 must be **high** to indicate that valid data is available. Checking the status register for available data is required before **every byte** read.

5.5.3.2 Device Register Read

After a write request to the device is made, 8 bytes of data is available to be read back. Use the single byte read process, as mentioned previously, to read all the bytes. See Section 4.2 for information of the exact number of request write bytes and the number of request read bytes, which is 8. All 8 bytes must be read to fully clear the transfer buffer; the first byte read is the most significant byte.

6 Calibration

6.1 Calibration EEPROM Map

Table 9 represents the EEPROM map of the device calibration values. All values are stored as little-endian 4-byte floating point numbers. Every point is 4-bytes long. Access to the data is possible through the CAL_EEPROM_READ register, which reads 8 bytes starting at the address pointed to by the register input.

Table 9. Calibration EEPROM Map

Offset address	Points	Length (Bytes)	Data Type	Description
0x00	664	664	U_8	Factory Reserved
0x298	1	4	Float_32	Calibration Temperature
0x29B	2	8	Float_32	Temp coeff C1, C2
0x2B8	3x8	96	Float_32	
0x338	22	88	Float_32	IF response cal frequencies 25, 50, 75, ..., 550 in MHz
0x390	22	88	Float_32	IF3_response, relative gain to 225 MHz at each calibration frequency for IF3_filter1 500 MHz filter
0x3E8	22	88	Float_32	IF3_response, relative gain to 225 MHz at each calibration frequency for IF3_filter1 250 MHz filter
0x5CC	30	120	Float_32	Relative If3_atten#1, 1-30 dB, 1 dB step
0x644	30	120	Float_32	Relative If3_atten#2, 1-30 dB, 1 dB step
0x6CC	1	4	Float_32	Relative Bypass IF3 gain, dB
0x6D0	1	4	Float_32	Relative Bypass IF3 1.25 GHz BPF gain
0x6D4	30	120	Float_32	Relative Bypass IF3_atten#2, 1-30 dB, 1 dB step
0x7D8	1	4	Float_32	Relative IF3_invert gain
0x7DC	1	4	Float_32	Relative IF2_Low BW gain
0x7E8	17	68	Float_32	Bypass Conv frequencies (start 50 MHz, 50 MHz steps to 850 MHz, 17 points) in MHz
0x82C	17	68	Float_32	Bypass Conversion Absolute gain at each freq
0x870	17x30	2040	Float_32	Bypass Relative IF3#2 atten at each freq. a1_f0, a1_f1,...,a1_fN a2_f0, a2_f1,...,a2_fN a30_f0, a30_f1,...,a30_fN

Offset address	Points	Length (Bytes)	Data Type	Description
0x1868	1	4	Float_32	IF2 ext absolute gain dB
0x186C	30	120	Float_32	Relative IF2ext Attenuator attenuation, 1-30 dB, 1 dB step
0x18F8	62	248	Float_32	RF calf req, 100-6200, every 100, in MHz
0x19F0	62	248	Float_32	RF absolute gain at every freq
0x1AE8	62	248	Float_32	Relative RF amp gain at every freq
0x1BE0	62x30	7440	Float_32	RF atten#1, 1-30 dB, 1 dB step for each freq a1_f0, a1_f1,...,a1_fN a2_f0, a2_f1,...,a2_fN a30_f0, a30_f1,...,a30_fN
0x38F0	62x30	7440	Float_32	RF atten#2, 1-30 dB, 1 dB step for each freq a1_f0, a1_f1,...,a1_fN a2_f0, a2_f1,...,a2_fN a30_f0, a30_f1,...,a30_fN

6.2 Absolute Conversion Gain

It is difficult to make gain measurements of every configuration setting of the downconverter as there are many combinations of attenuator and frequency settings, not to mention the various operating temperatures. However, the gain of the device can be computed to a reasonable level of accuracy with less data if the assumption is that every component setting is independent from one another. For example, assume the attenuator state of the IF3_ATTEN#1 does not affect the state of IF3_ATTEN#2, so with this independence there are only 2*30 attenuation measurements that need to be made; there is a mutually exclusive relationship. On the other hand, if they are not independent, for every setting of IF_ATTEN#1, 30 measurements are needed for IF3_ATTEN#2, bringing the total number of measurements to 30*30.

6.3 Absolute Gain of the RF Conversion Path

Assuming independency, and to be able to compute the gain of the downconverter at any setting, an absolute reference state of the device must be determined first. Once this reference state is established, compensation can be applied to other relative configured states of the device. The established reference state of the device is as follows:

- All attenuators are set to 0 dB
- IF2 Filter setting is 0, or 160 MHz filter selected
- IF3_Filter1 setting is 0, 500 MHz LPF selected

- IF3_Filter2 setting is 0, 1500 MHz LPF is selected
- IF3 bypass conversion is 0, RF is converted to by mixer 3
- IF frequency is set at 150 MHz
- RF is tuned from 100 MHz to 6200 MHz in 100 MHz steps

The gain of the device in this state is measured at different frequencies in the range of 100 MHz to 6.2 GHz. This set of measurements is the RF absolute gain stored at starting address 0x19F0 of the calibration EEPROM. All other measurements taken as deviations from this reference setting are relative.

6.4 Gain Through the Bypass RF Conversion Path

The absolute gain through the bypass path is stored beginning at address 0x82C. The absolute gain measurement is made every 50 MHz, between 50 MHz and 500 MHz.

6.4.1 Applying Calibration

The gain and attenuator values are relative measurements from the absolute reference values made over various RF frequencies. These relative values are either subtracted (attenuation) or added (gain) to the absolute gain value to determine the gain of the relative configuration. For example, assume the RF_ATTEN#1 is at 20 dB, IF3_ATTEN#1 is at 10 dB, IF2_Filter bank is set to select the 80 MHz filter, IF3 frequency is set to 140 MHz, and the RF frequency is set to 1.550 GHz. A possible systematic approach would be:

1. Compute the relative RF Atten#1 value by interpolation because there is no measurement value at 1.55 GHz. A simple linear interpolation between the measured 1.5 GHz and 1.6 GHz values would provide a good estimate. A local spline interpolation over 5-6 surrounding points would provide better accuracy. Let us call this value *rf_atten1*.
2. The IF3 Atten#1 attenuation value is read directly from memory; however, it must be corrected for frequency offset from 150 MHz. There are offset gain response values measured at 125 MHz and 150 MHz, so a simple linear interpolation between 2 points should be sufficient. Let us call this correct attenuation value *if3_atten1*.
3. The IF2 filter gain is read directly from memory, which we shall call *if2_filter*.
4. The absolute gain at the frequency can be determined using interpolation between 2 absolute gain points, which we shall call *G_abs*.
5. The gain for this configuration is calculated using:

$$G = G_{abs} + if_{filter} - rf_{atten1} - if3_{atten1}$$

If the current device temperature is different from the calibration temperature, the gain correction due to temperature difference is computed using

$$\Delta G_{temp} = C(b1)_1(T - T_0) + C(b1)_2(T - T_0)^2.$$

ΔG_{temp} is the gain correction, $C(b1)_1$ and $C(b1)_2$ are the first and second order temperature gain coefficients respectively for RF band 1, and T and T_0 are the current temperature and

calibration temperature respectively. Adding this correction to the previously calculated gain will compensate the value for temperature deviation.

$$G = G_{abs} + if_{filter} - rf_{atten1} - if_{3atten1} + \Delta G_{temp}$$

Revision Table

Revision	Revision Date	Description
1.0	1/15/17	Initial Release
1.1	5/12/17	Corrected Status parameters
1.2	6/13/19	Address removed
2.0	8/5/20	Updated formatting
2.1	12/7/22	Corrected torque range

